IN THE CLAIMS

1. (Original) A ferroelectric memory device comprising:

a lower interlayer insulating layer formed on a semiconductor substrate;

at least two adjacent ferroelectric capacitors disposed on the lower interlayer insulating layer;

an interlayer insulation layer formed over the ferroelectric capacitors, leaving a top surface of the ferroelectric capacitors exposed;

a patterned via etch-stop layer formed on the interlayer insulation layer, leaving the top surface of the capacitors exposed;

an upper interlayer insulating layer formed on the patterned via etch-stop layer; and

a plate line commonly connected to the at least two adjacent ferroelectric capacitors.

2. (Original) The ferroelectric memory device of claim 1, wherein the plate line contacts the patterned via etch-stop layer disposed between the at least two adjacent ferroelectric capacitors.

3. (Original) The ferroelectric memory device of claim 1, wherein the patterned via etch-stop layer is made of a material having a different etch selectivity from the interlayer insulation layer and the upper interlayer insulating layer.

4. (Original) The ferroelectric memory device of claim 1, wherein the interlayer insulation layer and the upper interlayer insulating layer comprise an oxide, and the patterned via etch-stop layer is made of a material layer selected from the group consisting of a titanium oxide layer, a silicon nitride layer, a silicon oxynitride layer, an aluminium oxide layer, and combinations thereof.

5. (Original) The ferroelectric memory device of claim 1, wherein the plate line contacts the upper electrodes of the at least two adjacent ferroelectric capacitors through a slit-shaped common via hole passing through the upper interlayer insulating layer.

6. (Original) The ferroelectric memory device of claim 1, further comprising an encapsulating barrier layer that covers the patterned via etch-stop layer to prevent permeation of hydrogen.

7. (Original) The ferroelectric memory device of claim 6, wherein the encapsulating barrier layer comprises a metal oxide layer selected from the group consisting of an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer, a silicon nitride layer, a cerium oxide layer, and combinations thereof.

8. (Original) The ferroelectric memory device of claim 1, wherein the upper interlayer insulating layer comprises:

a first upper interlayer insulating layer and a second upper interlayer insulating layer, which are sequentially stacked, and

strapping lines disposed between the first upper interlayer insulating layer and the second upper interlayer insulating layer, and placed adjacent the plate line.

9. (Original) The ferroelectric memory device of claim 1, wherein the lower interlayer insulating layer comprises:

a plurality of cell transistors disposed on the semiconductor substrate;

a plurality of bit lines electrically connected to drain regions of the cell transistors; and

a plurality of contact plugs electrically connected to source regions of the cell transistors,

wherein the ferroelectric capacitors electrically contact source regions through the contact plugs.

10. (Original) The ferroelectric memory device of claim 1, wherein the at least two adjacent ferroelectric capacitors each include a lower electrode, a ferroelectric layer pattern and an upper electrode layer, and wherein the plate line directly contacts the upper electrodes of the at least two adjacent ferroelectric capacitors.

11. (Original) The ferroelectric memory device of claim 5, wherein the interlayer insulation layer and the patterned via etch-stop layer define cell via holes that expose a top

surface of the ferroelectric capacitors, and the cell via holes overlap with the slit-shaped common via hole.

12. (Original) A ferroelectric memory device comprising:

a lower interlayer insulating layer formed on a semiconductor substrate;

at least two adjacent ferroelectric capacitors disposed on the lower interlayer insulating layer;

an interlayer insulation layer disposed between the ferroelectric capacitors and extending to substantially the same height as the ferroelectric capacitors, leaving a top surface of the ferroelectric capacitors exposed;

a patterned via etch-stop layer formed on the interlayer insulation layer, leaving a top surface of the interlayer insulation layer exposed between the at least two adjacent ferroelectric capacitors;

an upper interlayer insulating layer formed on the patterned via etch-stop layer; and

a plate line commonly connected to the at least two adjacent ferroelectric capacitors.

13. (Original) The ferroelectric memory device of claim 12, wherein the patterned via etch-stop layer is made of a material having a different etch selectivity from the interlayer insulation layer and the upper interlayer insulating layer.

14. (Original) The ferroelectric memory device of claim 13, wherein the interlayer insulation layer and the upper interlayer insulating layer comprise an oxide layer, and the patterned via etch-stop layer is made of a material layer selected from the group consisting of a titanium oxide layer, a silicon nitride layer, a silicon oxynitride layer, an aluminium oxide layer, and combinations thereof.

15. (Original) The ferroelectric memory device of claim 12, further comprising an encapsulating barrier layer formed between the ferroelectric capacitors and the interlayer insulation layer or within the upper interlayer insulating layer to prevent permeation of hydrogen.

16. (Original) The ferroelectric memory device of claim 15, wherein the encapsulating barrier layer comprises a metal oxide layer selected from the group consisting

of an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer, a silicon nitride layer, a cerium oxide layer, and combinations thereof.

17. (Original) The ferroelectric memory device of claim 12, wherein the at least two adjacent ferroelectric capacitors each include a lower electrode, a ferroelectric layer pattern and an upper electrode layer, and wherein the plate line is in direct contact with the upper electrodes of the at least two adjacent ferroelectric capacitors.

18. (Original) The ferroelectric memory device of claim 12, wherein the plate line is in contact with the at least two adjacent ferroelectric capacitors through a slit-shaped common via hole that passes through the upper interlayer insulating layer.

19. (Original) The ferroelectric memory device of claim 12, wherein the interlayer insulation layer is planarized.

20. (Currently amended) The ferroelectric memory device of claim ~~6~~ 15, wherein the encapsulating barrier layer comprises a metal oxide layer selected from the group consisting of an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer, a silicon nitride layer, a cerium oxide layer, and combinations thereof.